REMARKS

Applicants propose amending claims 1, 5, 8, 10, 12, 16-18, 21, 23-24, 26, 28, 30, and 33-34 and canceling claims 2-3, 11, 13, 19-20, 27, and 29. No new matter has been introduced by the proposed amendments. Applicants respectfully request that the proposed amendments be entered because the amendments are submitted to place the present application in better condition for allowance or appeal. Moreover, the proposed amendments merely incorporate material already claimed in one or more dependent claims into the independent claims and therefore do not present new issues requiring further consideration or search.

Pursuant to the proposed amendments, claims 1, 4-10, 12, 14-18, 21-26, 28, and 30-34 are pending in the present application. In the Office Action, claims 1-34 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Nagaraj, et al (U.S. Patent No. 5,805,842). Pursuant to the proposed amendments, the Examiner's rejections of claims 2-3, 11, 13, 19-20, 27, and 29 are rendered moot. The Examiner's remaining rejections are respectfully traversed.

With regard to independent claims 1 and 18, Applicants describe and claim a method and an apparatus, respectively, for executing a read request over a PCI bus. The method includes obtaining an access request from a queue, transferring, by a first DMA transfer, data from a time-variant main memory to a time-invariant second memory on a first device, and transferring, by a second DMA transfer, the data from the time-invariant second memory to a second device. The apparatus includes a queue for storing a read access request, the time-variant main memory for storing data to be transferred, and a time-invariant buffer memory for buffer storage of the data, whereby data transfer to the time-invariant buffer memory is accomplished by a first DMA transfer. The claimed apparatus also includes a device located on the PCI bus for receiving the data, whereby data transfer from the time-invariant buffer memory to the device is accomplished

by a second DMA transfer, and a finite state machine associated with the queue for selecting an access request.

With regard to independent claims 10 and 26, Applicants describe and claim a method and an apparatus, respectively, for executing a write request over a PCI bus. The method includes writing an access request to a queue, transferring, by a first DMA transfer, data from a second device to a time-invariant second memory on a first device, and transferring, by a second DMA transfer, the data from the time-invariant second memory to a time-variant main memory of the first device. The apparatus includes a queue for storing a write access request, a device located on a PCI bus for storing data to be transferred, and the time-variant main memory for receiving the data. The apparatus also includes a time-invariant buffer memory for buffer storage of the data, whereby data transfer to the time-invariant buffer memory is accomplished by a first DMA transfer and data transfer from the time-invariant buffer memory to the time-variant main memory is accomplished by a second DMA transfer, as well as a finite state machine associated with the queue for selecting an access request.

To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Applicants respectfully submit that Nagaraj fails to teach or suggest all the claim limitations.

Nagaraj is directed to enabling a Peripheral Component Interconnect (PCI) bus to support direct memory access (DMA) transfers. Nagaraj describes a Main Memory 210 coupled to a PCI bus 220, which is also coupled to a PCI I/O device 225 and a plurality of DMA devices 230a-n. The PCI I/O device 225 described by Nagaraj includes an internal storage element 340 and two DMA controllers 300, 310. See Nagaraj, Figures 2 and 3. In operation, the PCI I/O device 225

performs a DMA transfer operation, such as a read or a write, by splitting the DMA transfer operation into two PCI cycles, i.e. one memory cycle and one I/O cycle. See Nagaraj, col. 4, ll. 19-24.

However, Nagaraj appears to be completely silent with regard to the temporal properties of the Main Memory 210 and the internal storage element 340. In particular, Nagaraj does not teach that the Main Memory 210 is time-variant and the internal storage element 340 is time-invariant. Thus, Applicants respectfully submit that Nagaraj does not teach or suggest either a time-invariant buffer memory or a time-variant main memory, as claimed by Applicants in independent claims 1, 10, 18, and 26.

For at least the aforementioned reasons, Applicants respectfully submit that the cited reference does not teach or suggest all the limitations of independent claims 1, 10, 18, and 26. Applicants submit that independent claims 1, 10, 18, 26, and all claims depending therefore are not obvious over Nagaraj and request that the Examiner's rejections under 35 USC 103(a) be withdrawn.

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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